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Project Proposal

Exploring FPGA Interconnect Fabric through Mathematical Analysis and Simulation

Problem

In our project, we will be analyzing different structures for the interconnect of a Field Programmable Gate Array (FPGA), and then use our analysis to recommend a specific topology. A typical look-up-table-based FPGA architecture consists of configuration logic blocks (CLB) which contain a cluster of logic elements (BLE) each containing input LUT, Multiplexer and flipflops (FF). SRAM bits configure the connectivity of the CLB’s and the interconnect fabric between them to form paths. Each interconnect net connects CLB’s using one or more wire segments and crossbar switch boxes. Our project will be focused on finding the best topology for the switch boxes.

There are three main switch box structures that we will explore. The first is a tri-state inverter structure, which has been used before in FPGA structures. The second is a transmission-gate structure, which provides less area, but does not exhibit all of the same positive features a tri-state interconnect does, such as regeneration. A third option we will be looking into is a simpler pass gate structure, which promises to be most efficient in sub-vt [Joe’s Paper].

FPGAs caught our attention because we believe that they can prove to be very useful in the future, especially in ultra-low power applications. FPGAs are more energy efficient than the general purpose processors (GPPs) used today. While FPGAs are not as flexible as GPPs, they are more flexible than Application-specific integrated circuits (ASICs), which are the most efficient. FPGAs thus provide a middle ground, in which we can get the best of both worlds; adequate efficiency and flexibility [Flexible Circuits].

Approach

Our approach will be to test different FPGA-interconnect structures in two ways. The first will be through mathematical analysis. Using equations from this class, we will analyze the resistance, delay, and energy consumption of each structure. We will put these metrics in terms of some of the specifications of an FPGA interconnect that we can change (Supply voltage, Voltage of configuration bit, etc.) and create plots to show how each of the FPGA structures (tri-state buffer, transmission gate, and pass gate) behave over a range of values.

We will also look at the different interconnect structures through simulation. We will set up simulations using the TASE tool, which will allow us to run the same simulation in different technologies, or sizes/models of transistors. These will include simulating individual switches, long switch paths, and branching switch paths. These three examples provide a way to test almost the entire spectrum of possibilities for FPGA switch-box interconnects in three tests. The simulation data for all of these tests will be compared to the analytical data that we discussed earlier, and we hope to show which switch box topology will be best for a given application both analytically and through simulation.

Design

As mentioned, there will be three main switch box designs that we will be testing: the tri-state inverter switch, the transmission gate switch, and the passgate switch. There will be three main circuit simulations that we will be designing. The first will simply be the structure, stand alone. We will find the values of delay, resistance, and energy dissipated mathematically, and then use simulations to ideally verify those results. Next we will look at a long path of switches, up to around twenty. With this design, we will calculate the resistance, delay, and energy at different points along the path (2, 4, 10, and 20 stages) and compare them to simulation. Additionally, we will explore branching paths (1, 2, and 3 branches) and do a similar comparison between mathematical analysis and simulation.

For each of the tests, we will have different constraints with which we will work within. For example, typical wires of a 90-nm FPGA have a certain resistance (50 Ω), capacitance (13 fF), and length (100 um). Since we want to also include the parasitic capacitances of the switches (the transistors), we will be using 43 fF for the tri-state buffers and 27 fF for the transmission gates and passgates.

To establish which switch box is best (i.e. most efficient) we will be using Pareto curves, which plot Energy vs. Delay. We will create a plot for each switchbox structure, as well as one for each interconnect structure (single switch, long path, and branching path). Each curve will be dependent on the supply voltage.

VARIABILITY

Novelty

We believe that this will be a unique, exhaustive study of interconnect structure, both analytically and through simulation. We have seen other publications that propose different structures and show through simulation that they work, but we believe that it would be more convincing to provide mathematical support in addition to simulation data.

Expected Outcomes

At the conclusion of our project, we will have analytic expressions for delay, resistance, and energy in terms of the supply voltage for the different switch structures. We also plan to be able to use these analytic expressions to choose which switch box will be the best fit for different applications (for example, super- vs. sub-vt). Our simulation data will ideally match up with our analytical data, and we will have two ways of showing the best choices for FPGA interconnect structures. Our hunch currently is that the passgate topology will minimize delay and energy in super- and sub-vt applications. We believe that because the passgates use much fewer transistors (1) than a tri-state buffer, for example, the resistance will be much lower, and therefore so will the delay and the energy. Because current has a linear dependence on voltage in super-vt and an exponential dependence in sub-vt, we believe that the passgate will save even more power and have less delay in the sub-vt operating region.

Preliminary Simulation

1. Tri-state buffer – 20-switch path

We simulated an FPGA interconnect path that goes through 20 switches before the signal terminates. Each of the switches is a tri-state inverter. Each inverter is enabled, and the input signal is a buffered square wave with a period of 5 ns.

After simulating for 20 ns (4 periods), we calculated the delay in the signal after 2, 4, 10 and 20 switches. We found that the delay increased with the number of switch boxes (to be expected), and that the increase is almost exactly linear according to the simulation. The graph is shown below:



While we got good results from the simulation, it isn’t quite indicative of the FPGA structure we are looking to assess. The constraints for our simulation, particularly those pertinent to the wires (capacitance, resistance, length and length) were typical values for FPGAs fabricated in 130 nm CMOS technology. The work we want to do will be in 90 nm technology, and then using the TASE tool we can generalize our simulations for any technology.

Group Breakdown

Analytical Exploration:

Seyi – Sub-vt equations

Pooja – Super-vt equations

Simulations – Together

Timeline

By 10/21 – Resistance, delay, and Energy calculations and simulations for Tristate buffer

By 10/28 – Resistance, delay, and Energy calculations and simulations for Transmission Gate

By 11/04 - Resistance, delay, and Energy calculations and simulations for Passgates

By 11/08 – Formal Design Review II

By 11/15 – Debugging of simulations as a result of Design Review II

By 11/28 – Complete simulations, data collection, and plots

By 12/01 – Final Report and Presentation